

#### DISTINCTIVE CHARACTERISTICS

- Five independent 16-bit counters
- High speed counting rates
- Up/down and binary/BCD counting
- Internal oscillator frequency source
- Tapped frequency scaler
- Programmable frequency output
- 8-bit or 16-bit bus interface
- Time-of-day option
- Alarm comparators on counters 1 and 2
- Complex duty cycle outputs
- One-shot or continuous outputs
- Programmable count/gate source selection
- Programmable input and output polarities
- Programmable gating functions
- Retriggering capability
- +5 volt power supply
- Standard 40-pin package
- 100% MIL-STD-883 reliability assurance testing

#### GENERAL DESCRIPTION

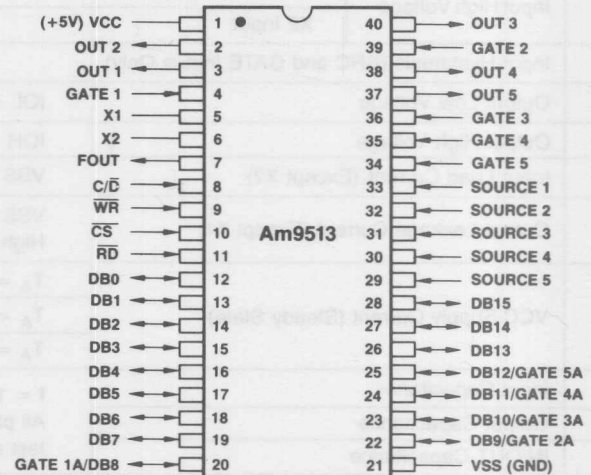
The Am9513 System Timing Controller is an LSI circuit designed to service many types of counting, sequencing and timing applications. It provides the capability for programmable frequency synthesis, high resolution programmable duty cycle waveforms, retriggerable digital one-shots, time-of-day clocking, coincidence alarms, complex pulse generation, high resolution baud rate generation, frequency shift keying, stop-watching timing, event count accumulation, waveform analysis and many more. A variety of programmable operating modes and control features allow the Am9513 to be personalized for particular applications as well as dynamically reconfigured under program control.

The STC includes five general-purpose 16-bit counters. A variety of internal frequency sources and external pins may be selected as inputs for individual counters with software selectable active-high or active-low input polarity. Both hardware and software gating of each counter is available. Three-state outputs for each counter provide pulses or levels and can be active-high or active-low. The counters can be programmed to count up or down in either binary or BCD. The host processor may read an accumulated count at any time without disturbing the counting process. Any of the counters may be internally concatenated to form any effective counter length up to 80 bits.

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#### CONNECTION DIAGRAM



Top View

Pin 1 is marked for orientation.

Figure 1.

MOS-172

#### ORDERING INFORMATION

Package Type	Temperature Range	Counting Frequency
		7MHz
Molded	$0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$	AM9513PC
Hermetic		AM9513DC
Hermetic	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	AM9513DM

**MAXIMUM RATINGS** beyond which useful life may be impaired

Storage Temperature	-65°C to +150°C
Ambient Temperature Under Bias	-55°C to +125°C
VCC with Respect to VSS	-0.5V to +7.0V
All Signal Voltages with Respect to VSS	-0.5V to +7.0V
Power Dissipation (Package Limitation)	1.5W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

**OPERATING RANGE**

Part Number	Temperature	VCC	VSS
Am9513DC/PC	0°C ≤ T <sub>A</sub> ≤ +70°C	+5V ±5%	0V
Am9513DM	-55°C ≤ T <sub>A</sub> ≤ +125°C	+5V ±5%	0V

**ELECTRICAL CHARACTERISTICS** over operating range (Notes 1 and 2)

Parameter	Description	Test Conditions	Min	Typ	Max	Units
VIL	Input Low Voltage	All Inputs Except X2	VSS - 0.5		0.8	Volts
		X2 Input	VSS - 0.5		0.8	
VIH	Input High Voltage	All Inputs Except X2	2.2V		VCC	Volts
		X2 Input	3.8		VCC	
VITH	Input Hysteresis (SRC and GATE Inputs Only)		0.2	0.3		Volts
VOL	Output Low Voltage	IOL = 3.2mA			0.4	Volts
VOH	Output High Voltage	IOH = -200μA	2.4			Volts
IIX	Input Load Current (Except X2)	VSS ≤ VIN ≤ VCC			±10	μA
IOZ	Output Leakage Current (Except X1)	VSS + 0.4 ≤ VOUT ≤ VCC High Impedance State			±25	μA
ICC	VCC Supply Current (Steady State)	T <sub>A</sub> = -55°C			275	mA
		T <sub>A</sub> = 0°C			255	
		T <sub>A</sub> = +25°C		190	235	
CIN	Input Capacitance	f = 1MHz, T <sub>A</sub> = +25°C, All pins not under test at 0V.			10	pF
COUT	Output Capacitance				15	
CIO	IN/OUT Capacitance				20	

**SWITCHING CHARACTERISTICS** over operating range (Notes 2, 3, 4)

**Am9513**

Parameter	Description	Figure	Min	Max	Min	Max	Units
TAVRL	C/D Valid to Read Low	23	25				ns
TAVWH	C/D Valid to Write High	23	170				ns
TCHCH	X2 High to X2 High (X2 Period)	24	145				ns
TCHCL	X2 High to X2 Low (X2 High Pulse Width)	24	70				ns
TCLCH	X2 Low to X2 High (X2 Low Pulse Width)	24	70				ns
TDVWH	Data In Valid to Write High	23	80				ns
TEHEH	Count Source High to Count Source High (Source Cycle Time) (Note 10)	24	145				ns
TEHEL TELEH	Count Source Pulse Duration (Note 10)	24	70				ns
TEHJV	Count Source High to FOUT Valid (Note 10)	24		500			ns
TEHGV	Count Source High to Gate Valid (Level Gating Hold Time) (Notes 10, 12, 13)	24	10				ns
TEHRL	Count Source High to Read Low (Set-up Time) (Notes 5, 10)	23	190				ns
TEHWH	Count Source High to Write High (Set-up Time) (Notes 6, 10)	23	100				ns
TEHYV	Count Source High to Out Valid (Note 10)	TC Output	24		300		ns
		Immediate or Delayed Toggle Output	24		300		
		Comparator Output	24		350		
TFN	FN High to FN+1 Valid (Note 14)	24		75			ns
TGVEH	Gate Valid to Count Source High (Level Gating Set-up Time) (Notes 10, 12, 13)	24	100				ns
TGVGV	Gate Valid to Gate Valid (Gate Pulse Duration) (Notes 11, 13)	24	145				ns
TGVWH	Gate Valid to Write High (Notes 6, 13)	23	0				ns
TRHAX	Read High to C/D Don't Care	23	0				ns
TRHEH	Read High to Count Source High (Notes 7, 10)	23	0				ns
TRHQX	Read High to Data Out Invalid	23	10				ns
TRHQZ	Read High to Data Out at High Impedance (Data Bus Release Time)	23		85			ns
TRHRL	Read High to Read Low (Read Recovery Time)	23		1000			ns
TRHSH	Read High to CS High (Note 15)	23	0				ns
TRHWL	Read High to Write Low (Read Recovery Time)	23		1000			ns
TRLQV	Read Low to Data Out Valid	23		160			ns
TRLQX	Read Low to Data Bus Driven (Data Bus Drive Time)	23	20				ns
TRLRH	Read Low to Read High (Read Pulse Duration) (Note 15)	23	160				ns
TSLRL	CS Low to Read Low (Note 15)	23	20				ns
TSLWH	CS Low to Write High (Note 15)	23	170				ns
TWHAX	Write High to C/D Don't Care	23	0				ns
TWHDX	Write High to Data In Don't Care	23	20				ns
TWHEH	Write High to Count Source High (Notes 8, 10, 17)	23	400				ns
TWHGV	Write High to Gate Valid (Notes 8, 13, 17)	23	400				ns
TWHRL	Write High to Read Low (Write Recovery Time)	23		1500			ns
TWHSH	Write High to CS High (Note 15)	23	20				ns
THWL	Write High to Write Low (Write Recovery Time)	23		1500			ns
TWHYV	Write High to Out Valid (Note 9, 17)	23		650			ns
TWLWH	Write Low to Write High (Write Pulse Duration) (Note 15)	23	150				ns

**The International Standard of Quality**  
guarantees these electrical AQLs on all  
parameters over the operating tempera-  
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0.2% on Bipolar Logic & Interface; 0.3%  
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